Amendments to the Specification:

Please replace the first three paragraphs of the specification with the following paragraphs:

The present application is a divisional of U.S. Patent Application Serial No. 10/205,735, filed July 26, 2002 (Docket No. 13439US04), which is a continuation of U.S. Patent Application Serial No. 09/437,719, filed November 9, 1999, now U.S. Patent 6,477,200, which claims priority on the basis of the following provisional applications: Serial Number 60/130,616 entitled “Multi-Pair Gigabit Ethernet Transceiver” filed on April 22, 1999, Serial Number 60/116,946 entitled “Multiple Decision Feedback Equalizer” filed on January 20, 1999, Serial Number 60/108,648 entitled “Clock Generation and Distribution in an Ethernet Transceiver” filed on November 16, 1998, Serial Number 60/108,319 entitled “Gigabit Ethernet Transceiver” filed on November 13, 1998, Serial Number 60/107,874 entitled “Apparatus for an Method of Distributing Clock Signals in a Communication System” filed November 9, 1998, and Serial Number 60/107,880 entitled “Apparatus for and Method of Reducing Power Dissipation in a Communication System” filed November 9, 1998.

The present application is related to the following co-pending applications, commonly owned by the assignee of the present application, the entire contents of each of which are expressly incorporated herein by reference: Serial Number 09/370,370, now U.S. Patent 6,253,345, issued June 26, 2001, entitled “System and Method for Trellis Decoding in a Multi-Pair Transceiver System”, Serial Number 09/370,353, now U.S. Patent 6,226,332, issued May 1, 2001, entitled “Multi-Pair Transceiver Decoder System with Low Computation Slicer”, Serial Number 09/370,354, now U.S. Patent 6,249,544, issued June 19, 2001, entitled “System and Method for High Speed Decoding and ISI Compensation in a Multi-Pair Transceiver System” Serial Number 09/370,491, now U.S. Patent 6,252,904, issued June 26, 2001, entitled “High-Speed Decoder for Multi-Pair Gigabit Transceiver”, all filed October 10, 1999, and Serial Number 09/390,856, now U.S. Patent 6,289,047, issued September 11, 2001, entitled “Dynamic ~~r~~Regulation of Power Consumption in a High-Speed Communication System” filed September 3, 1999.

The present application is also related to the following co-pending applications, filed on instant date herewith and commonly owned by the assignee of the present application, the entire contents of each of which are expressly incorporated herein by reference: Serial Number 09/437,721, now U.S. Patent 6,363,129, issued March 26, 2002, entitled "Timing Recovery System for a Multi-Pair Gigabit Transceiver" and Serial Number 09/437,724, now U.S. Patent 6,307,905, issued October 23, 2001, entitled "Switching Noise Reduction in a Multi-Clock Domain Transceiver".